In the Claims:

Please amend claims 3, 8-10 and 13 as indicated below. This listing of claims replaces all prior versions.

1. (Previously Presented) A method of coupling a plurality of test access port (TAP) controllers to a single external interface, comprising:

a) resetting a first bit in each of a plurality of TAP controllers to a known state;

b) producing a first signal based, at least in part, on the state of the first bit in each of the plurality of TAP controllers;

c) selecting one of the plurality of TAP controllers based, at least in part, on the first signal;

d) coupling an external input terminal to an input terminal of the selected one of the plurality of TAP controllers; and

e) coupling an output terminal of the selected one of the plurality of TAP controllers to an external output terminal.

2. (Original) The method of claim 1, wherein the TAP controller comprises a finite state machine and a plurality of registers.

3. (Currently Amended) The method of claim 2, further comprising entering a run-test-idle state by toggling the first bit in the selected one of the plurality of TAP controllers; and

while in the run-test-idle state,

selecting a second one of the plurality of TAP controllers based on the state of the first bit in each of the plurality of TAP controllers;

coupling the external input terminal to an input terminal of the second TAP controller; and

coupling an output terminal of the second TAP controller to the external output terminal ~~and repeating steps (b) through (e)~~.

4. (Previously Presented) The method of claim 3, further comprising providing a clock signal, a test mode selection signal, and a test reset signal to each of the plurality of TAP controllers.

5. (Original) The method of claim 3, wherein the plurality of TAP controllers are disposed on a single integrated circuit.

6. (Original) The method of claim 5, wherein the first signal is produced within the single integrated circuit.

7. (Original) The method of claim 6, further comprising receiving, from a source external to the single integrated circuit, a clock signal.

8. (Currently Amended) An integrated circuit, comprising:

a plurality of functional blocks, each functional block having a test access port (TAP) controller coupled thereto;

each TAP controller including a first register bit, each first register bit adapted to produce a known output state in response to a reset signal, each first register bit further adapted to toggle in response to a register write operation; and

routing logic adapted to selectively provide, based at least in part on the state of the plurality of first register bits, a communication path between an external input signal source and an input terminal of a selected one of the TAP controllers, the routing logic further adapted to provide, in response to toggling of the first register bit in the selected TAP controller and based on the state of each of the first register bits, a communication path between the external input signal source and an input terminal of a second one of the TAP controllers.

9. (Currently Amended) The integrated circuit of claim 8, wherein the routing logic is further adapted to selectively provide, based at least in part on the state of the plurality of first register bits, a communication path between an external output terminal and an output terminal of the selected ~~on the~~ TAP controllers, and the routing logic is further

adapted to provide, in response to the toggling of the first register bit in the selected TAP controller and based on the state of each of the first register bits, a communication path between the external output terminal and an output terminal of the second TAP controller.

10. (Currently Amended) The integrated circuit of claim 8, wherein at least one TAP controller further includes a second register bit; wherein the routing logic is further adapted to provide the output of a first TAP controller as an input to a second TAP controller, based at least in part on the state of the first and second register bits.

11. (Original) The integrated circuit of claim 9, wherein a transition between the selectively provided communication paths is transparent to an external observer.

12. (Previously Presented) An integrated circuit (IC), comprising:

a plurality of test access port (TAP) controllers disposed on the IC, each of the plurality of TAP controllers having a first input terminal adapted to receive a data input signal and an output terminal adapted to provide a data output signal, each of the plurality of TAP controllers further having at least one switch bit;

a first interface to receive an externally supplied input signal;

a second interface to transmit an internally generated output signal; and

routing logic adapted to selectively provide, based at least in part on the state of the switch bits of the plurality of TAP controllers, a first communication path between the input terminal of a predetermined one of the plurality of TAP controllers and the first interface, and a second communication path between the output terminal and the second interface.

13. (Currently Amended) The integrated circuit of claim 12, further comprising a plurality of functional blocks coupled respectively to each of the plurality of TAP controllers, wherein the routing logic is further adapted to provide, in response to toggling of the switch bit in the predetermined TAP controller and based on the state of each of the switch bits, a first communication path between the input terminal of a second

one of the plurality of TAP controllers and the first interface, and a second communication path between the output terminal of the second TAP controller and the second interface.

14. (Original) The integrated circuit of claim 13, wherein the each of the plurality of TAP controllers has a second input terminal adapted to receive a clock signal, a third input terminal adapted to receive mode select signal, and a fourth input terminal adapted to receive a reset signal; wherein the plurality of second input terminals are coupled in common, the plurality of third input terminals are coupled in common, and the plurality of fourth input terminals are coupled in common.

15. (Original) The integrated circuit of claim 14, further comprising a chain bit disposed in a first one of the plurality of TAP controllers.